In the Specification:

Page 1, paragraph beginning at line 2, has been rewritten as indicated below:

A1

The present invention relates to a semiconductor integrated circuit device, and more particularly to a semiconductor integrated circuit device which may be operated at both high speed and low electric power.

Page 1, paragraph beginning at line 7 and continuing through page 2, has been rewritten as indicated below:

A2

In order to improve the performance of semiconductor integrated circuit devices composed of CMOS circuits, some methods have been proposed such as shrinkage of MOS transistors that are a components of the CMOS circuitry, lowering of absolute values of threshold voltages of the MOS transistors, and raising of a supply voltage. In actuality, however, with improvement of an operating speed of the CMOS circuit, the power consumption is increased accordingly. For example, as the threshold voltage of the MOS transistor is made lower and lower, the operating speed becomes higher and higher, but the leak current is also increased. Likewise, with enhancement of the supply voltage, the operating speed is improved but the operation power is increased as well. The increase of the power consumption gives rise to disadvantages of degrading the circuit performance and bringing about an erroneous operation. The heat caused by the increase of the power consumption has the adverse effect on the mount of the semiconductor integrated circuit device, which disadvantageously leads to enhancing the manufacturing cost. Therefore, faster operation and lower power consumption have been significant issues to improving the performance of the CMOS circuit.